Analog to Digital Converters

David Andrews
dandrews@uark.edu

Slides adapted from:
ee.nmt.edu/~rison/ee308_spr02/020306.pdf
Ume.gatech.edu/mechatronics_course/ADC_F08.pdf

What is an A/D Converter ?

- Analog signals are continuous and directly measurable.
- Digital signals are discrete and only have two states {0 ,1}.
- An A/D transforms (maps) the analog continuous signal to a digital discrete form.

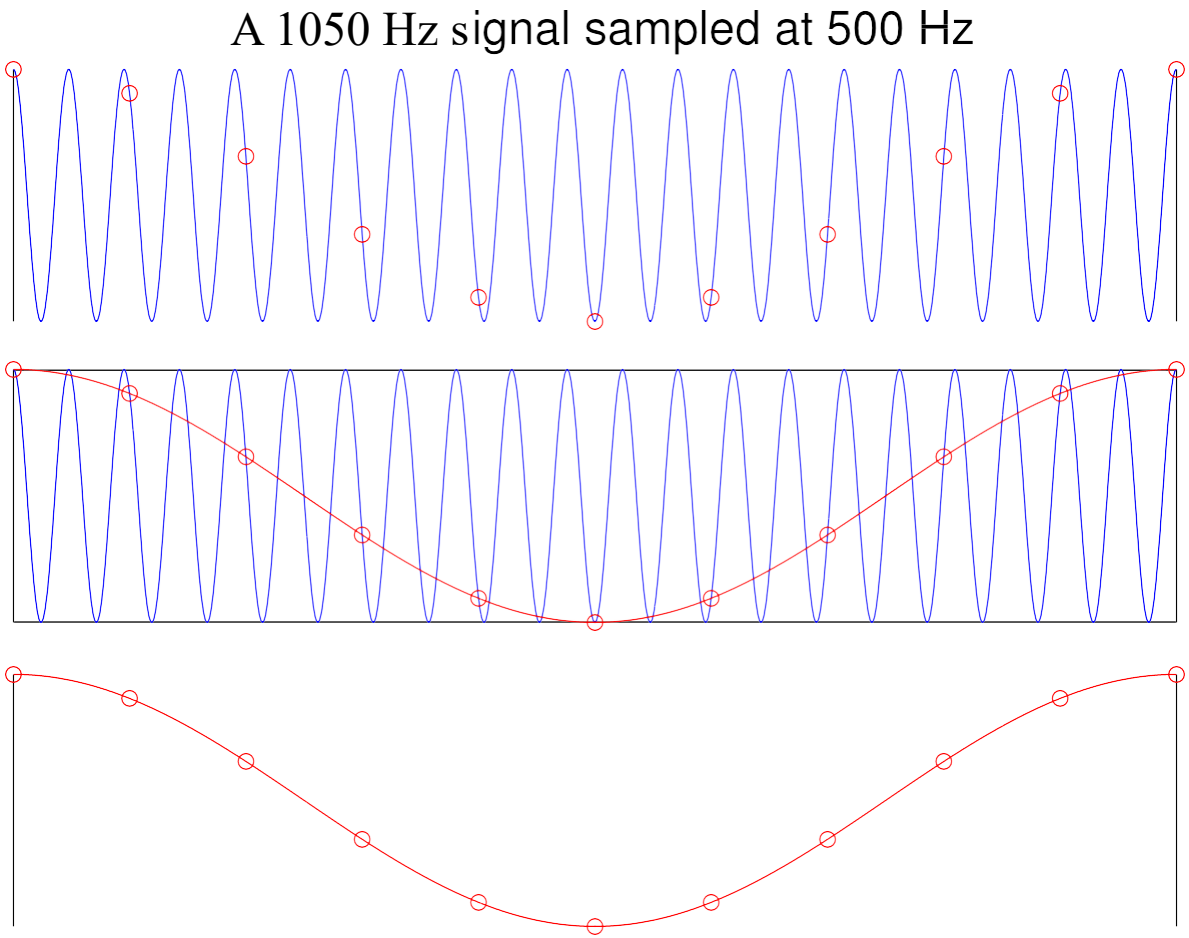
Practical Considerations

- How fast do we need to Sample ?
  - Signal Processing gives the answer
- What is the range of values $V_{hi} - V_{lo}$?
  - Resolution of digital representation
- What error can the system tolerate ?
  - Quantization error

How do A/D's Operate ?

- Several choices
  - We will study two:
  - Flash A/D's:
    - Fastest but most expensive
    - Practical limitations on resolution (#bits)
  - Successive Approximation
    - Slower than flash but still fast and cheaper
    - Higher resolution (#bits)
- Interestingly both built on D/A components
  - Analog Comparators, resistor trees

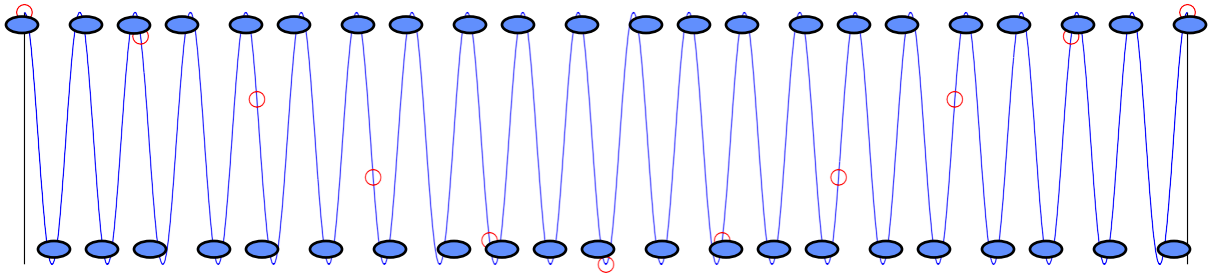
Sampling Rate (How fast)



The 1050 Hz signal looks like a 50 Hz signal !

Sampling Rate (How fast)

A 1050 Hz signal sampled at 500 Hz



Nyquist Rate:
Need to sample at least 2x faster than highest frequency

For (pure tone) 1050 Hz, minimum sampling rate = 2100 Hz

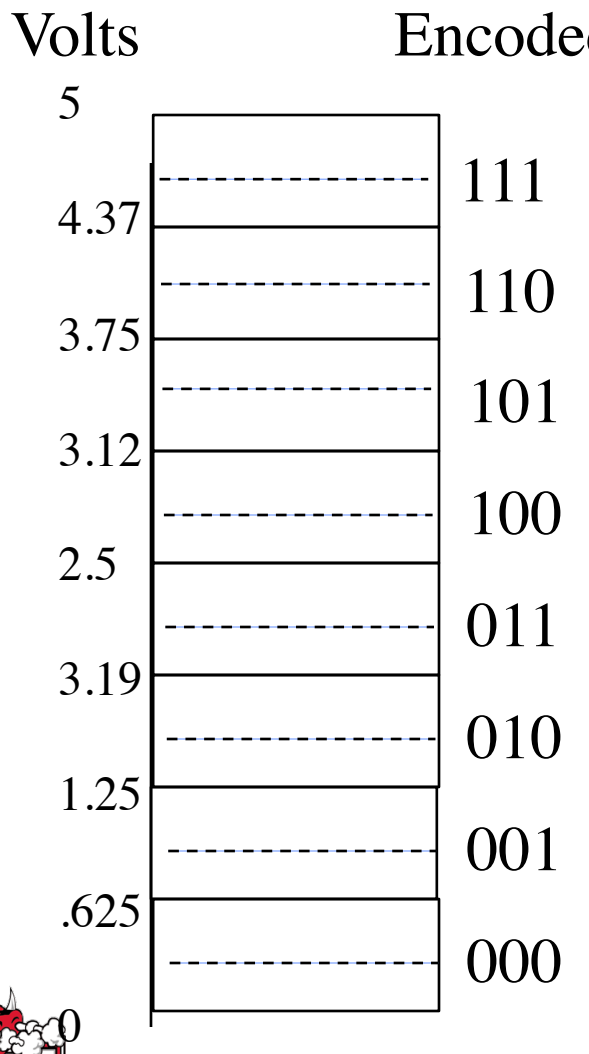
Rule of thumb: sample at 4x - 10x highest frequency

Quantization Error

- Resolution := #bits
- 3 bit resolution gives
  - 2^3 = 8 quantization levels
- Assume you are sampling a signal between 5volts – 0 volts

$$\frac{5v - 0v}{8} = .625v$$

Quantization Error



values between 4.37 – 5 = 111

values between 3.75 – 4.37 = 110

0

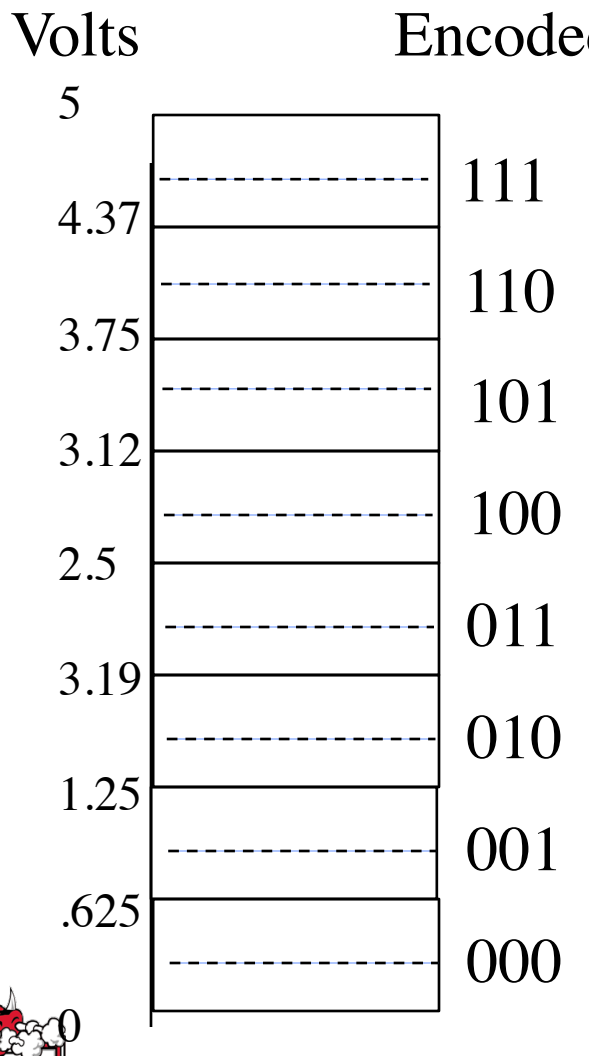
0

0

values between 1.25 – .625 = 001

values between .625 – 0 = 000

Quantization Error



$$\text{Error} \pm \frac{1}{2} \Delta$$

$$\frac{.625}{2} = \pm .3125\text{v}$$

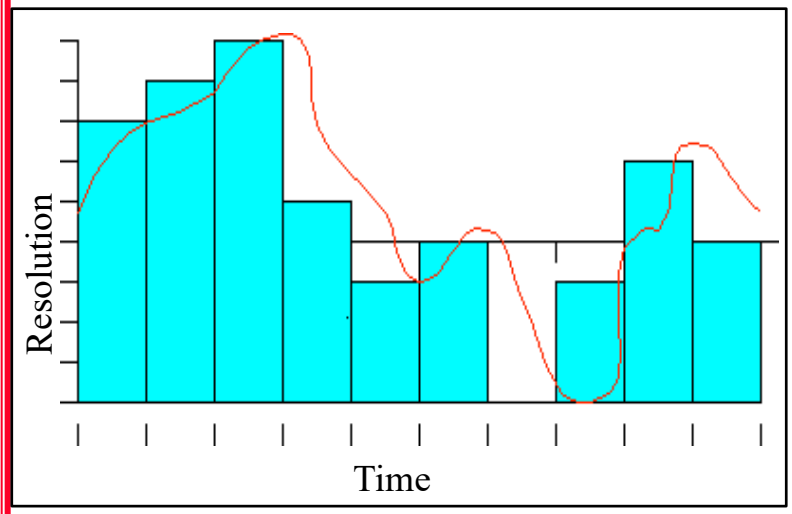
Accuracy of A/D Conversion

Two ways to improve the accuracy of A/D conversion:

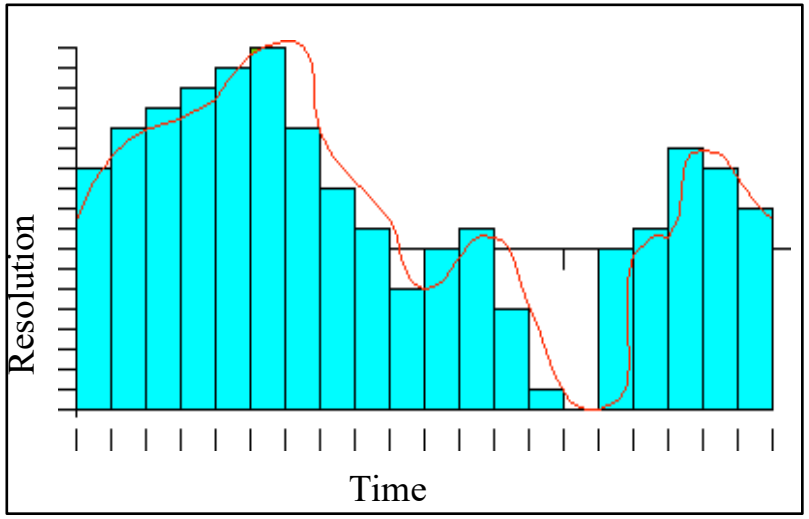
1. increasing the resolution which improves the accuracy in measuring the amplitude of the analog signal.
2. increasing the sampling rate which increases the maximum frequency that can be measured.

Accuracy of A/D Conversion

- Low Accuracy



- Improved



Meet the Comparator !

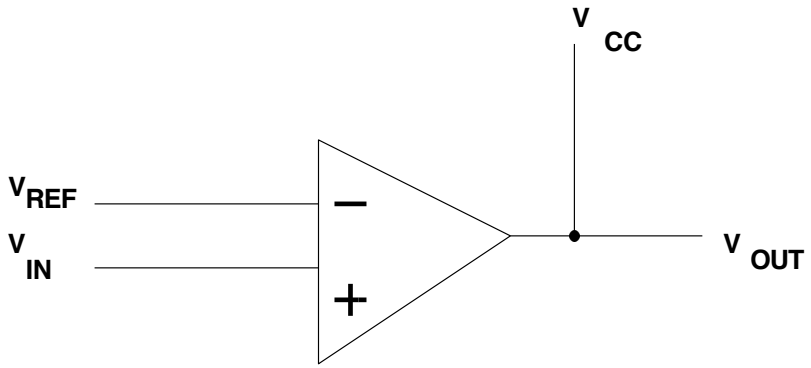
A comparator is used in many types of A/D converters.

A comparator is the simplest interface from an analog signal to a digital signal

Compares two voltage values on its two inputs

If the voltage on the + input is greater than the voltage on the - input, the output will be a logic high (1)

If the voltage on the + input is less than the voltage on the - input, the output will be a logic low (0)



If Vin > Vref then Vout = Vcc

If Vin < Vref then Vout = 0

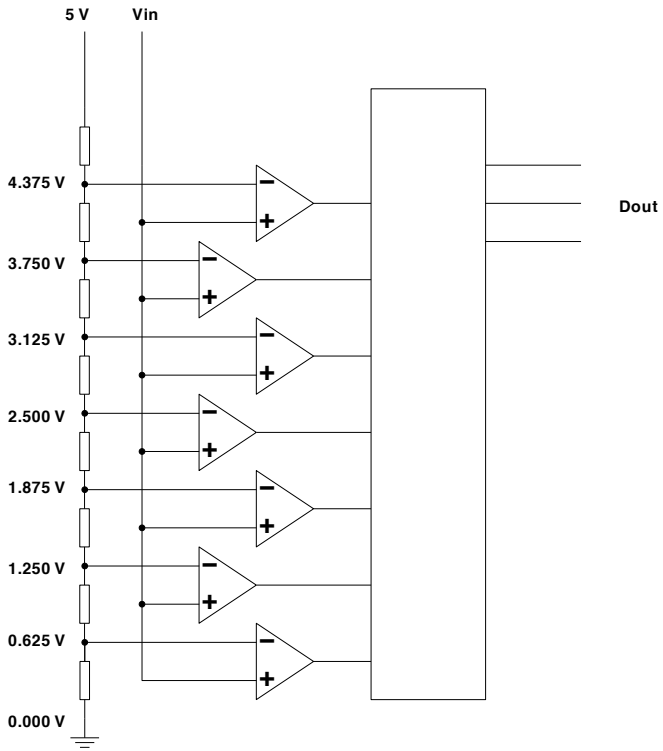
Flash (Parallel) A/D Converter

A flash A/D converter simplest to understand

A flash A/D converter compares an input voltage to a large number of reference voltages

An *n*-bit flash converter uses 2^n -1 comparators

The output of the A/D converter is determined by which of the two reference voltages the input signal is between



3-bit A/D converter

Flash A/D Converter

An n-bit Flash A/D converter requires 2^n -1 comparators

- 8-bit Flash A/D requires 255 comparators
- 12-bit Flash A/D converter would require 4,095 comparators
- Cannot integrate 4,095 comparators onto an IC The largest flash A/D converter is 8 bits

Flash A/D converters can sample at several billion samples/sec

Successive Approximation

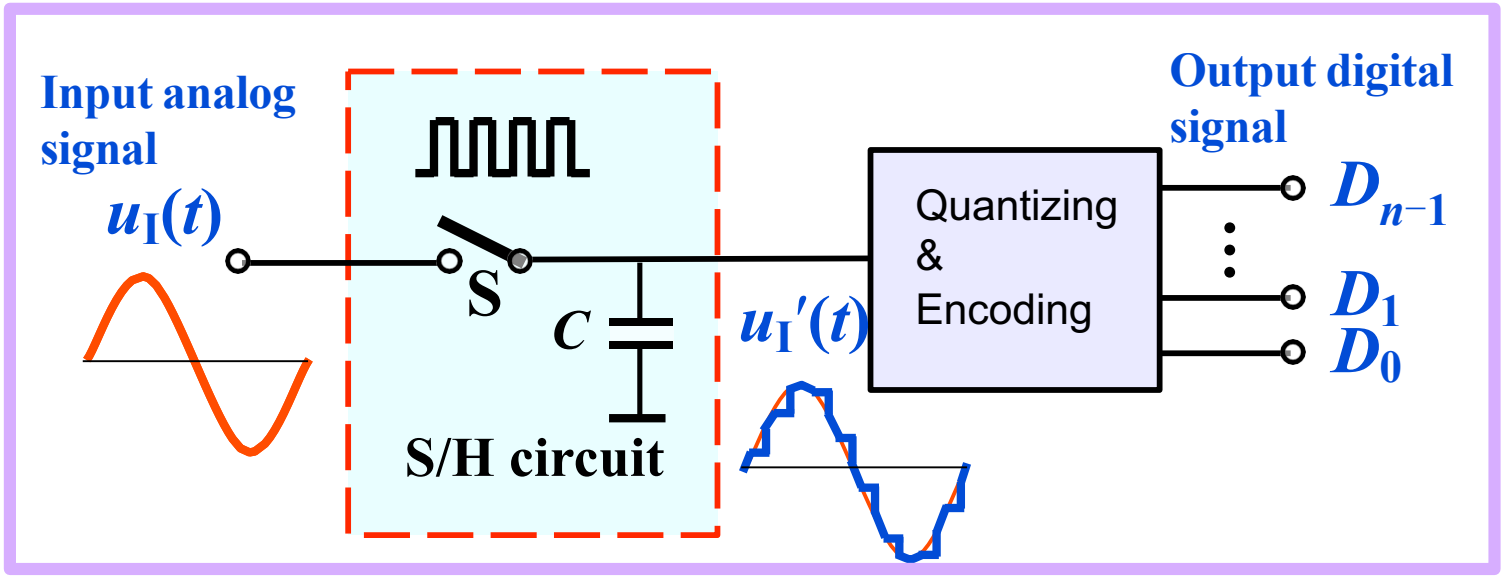
- A successive approximation (SA) A/D converter uses an intelligent scheme to determine the input voltage

- It first tries a voltage halfway between V_{max} and V_{min}. Determines if the signal is in the lower half or the upper half of the voltage range
  - If the input is in the upper half of the range, it sets the most significant bit of the output
  - If the input is in the lower half of the range, it clears the most significant bit of the output

- The first clock cycle eliminates half of the possible values
  - On the next clock cycle, the SA A/D tries a voltage in the middle of the remaining possible values
  - The second clock cycle allows the SA A/D to determine the second most significant bit of the result
  - Each successive clock cycle reduces the range another factor of two

For an n-bit SA A/D converter, takes n clock cycles to determine value

Successive Approximation

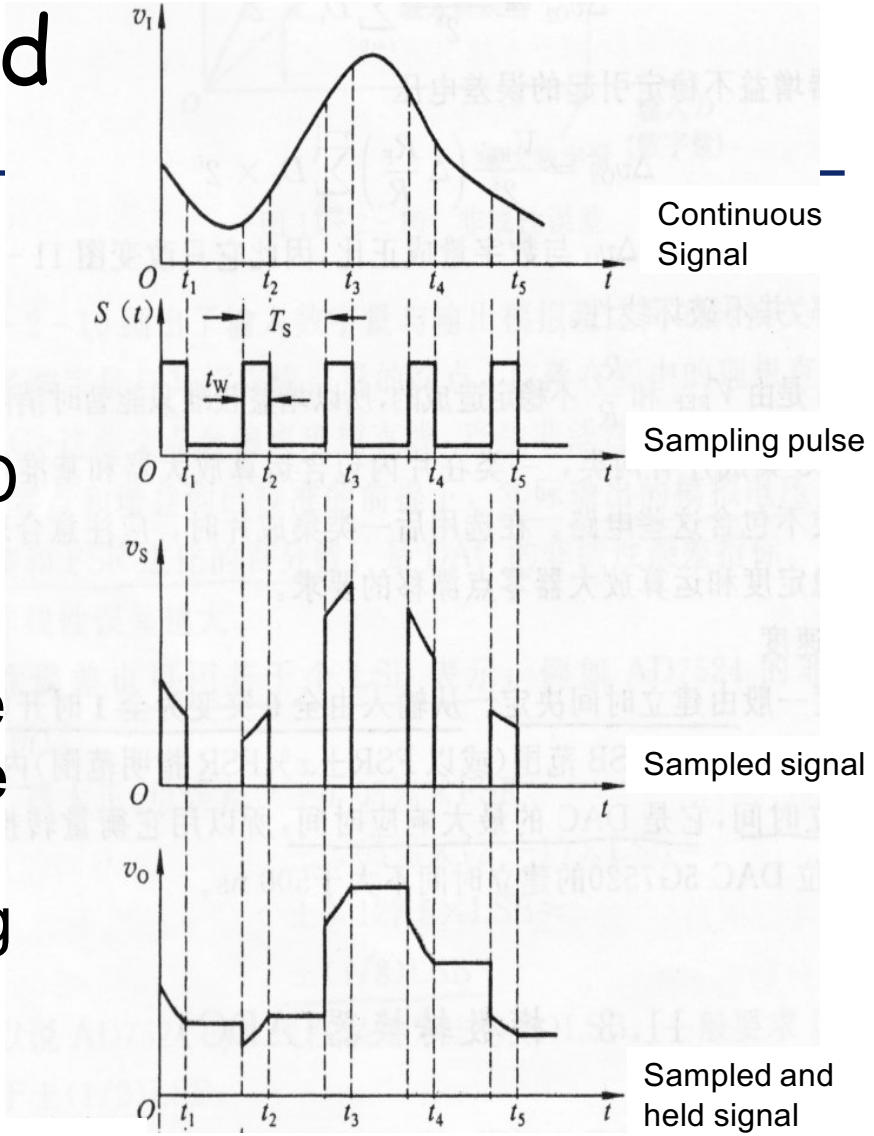


2 steps

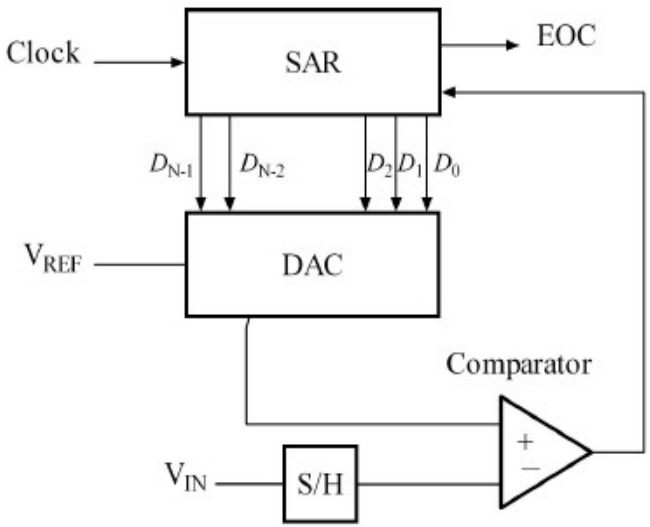
- Sampling and Holding (S/H)
- Quantizing and Encoding (Q/E)

Sampling and Holding

- Holding signal benefits the accuracy of the A/D conversion
- Minimum sampling rate should be at least twice the highest data frequency of the analog signal



Successive Approximation ADC Circuit



- Uses a n-bit DAC to compare DAC and original analog results.
- Uses Successive Approximation Register (SAR) supplies an approximate digital code to DAC of Vin.
- Comparison changes digital output to bring it closer to the input value.
- Uses Closed-Loop Feedback Conversion

Successive Approximation Example

Example

- 10 bit ADC
- Vin= 0.6 volts (from analog device)
- V_{ref}=1 volts
- Find the digital value of Vin

Bit	Voltage
9	.5
8	.25
7	.125
6	.0625
5	.03125
4	.015625
3	.0078125
2	.00390625
1	.001952125
0	.0009765625

$N=2^n$ (N of possible states)
N=1024
Vmax-Vmin/N = 1 Volt/1024 = 0.0009765625V of Vref (resolution)

Successive Approximation

- MSB (bit 9)
  - Divided V_{ref} by 2
  - Compare $V_{ref}/2$ with V_{in}
  - If V_{in} is greater than $V_{ref}/2$, turn MSB on (1)
  - If V_{in} is less than $V_{ref}/2$, turn MSB off (0)
  - V_{in} =0.6V and V=0.5
  - Since V_{in}>V, MSB = 1 (on)

Bit	Voltage
9	.5
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7	.125
6	.0625
5	.03125
4	.015625
3	.0078125
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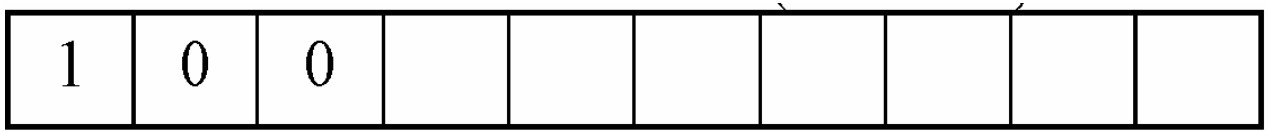
1	.001952125
0	.0009765625

Successive Approximation

- Next Calculate MSB-1 (bit 8)
  - Compare V_{in}=0.6 V to V=V_{ref}/2 + V_{ref}/4= 0.5+0.25 =0.75V
  - Since 0.6<0.75, MSB is turned off
- Calculate MSB-2 (bit 7)
  - Go back to the last voltage that caused it to be turned on (Bit 9) and add it to V_{ref}/8, and compare with V_{in}
  - Compare V_{in} with (0.5+V_{ref}/8)=0.625
  - Since 0.6<0.625, MSB is turned off



Successive Approximation

- Calculate the state of MSB-3 (bit 6)
  - Go to the last bit that caused it to be turned on (In this case MSB-1) and add it to $V_{ref}/16$, and compare it to V_{in}
  - Compare V_{in} to $V = 0.5 + V_{ref}/16 = 0.5625$
  - Since 0.6>0.5625, MSB-3=1 (turned on)

MSB	MSB-1	MSB-2	MSB-3	…					
1	0	0	1						

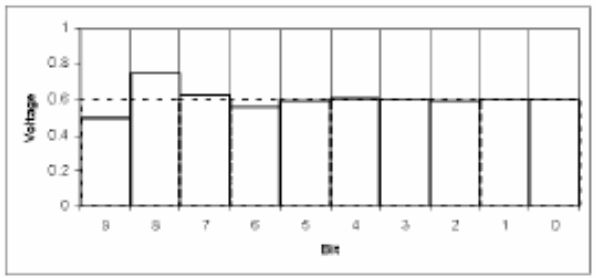
Successive Approximation ADC

- This process continues for all the remaining bits.

•Digital Results:

MSB	MSB-1	MSB-2	MSB-3	…					LSB
1	0	0	1	1	0	0	1	1	0

•Results: $\frac{1}{2}+\frac{1}{16}+\frac{1}{32}+\frac{1}{256}+\frac{1}{512}=.599609375$ V

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