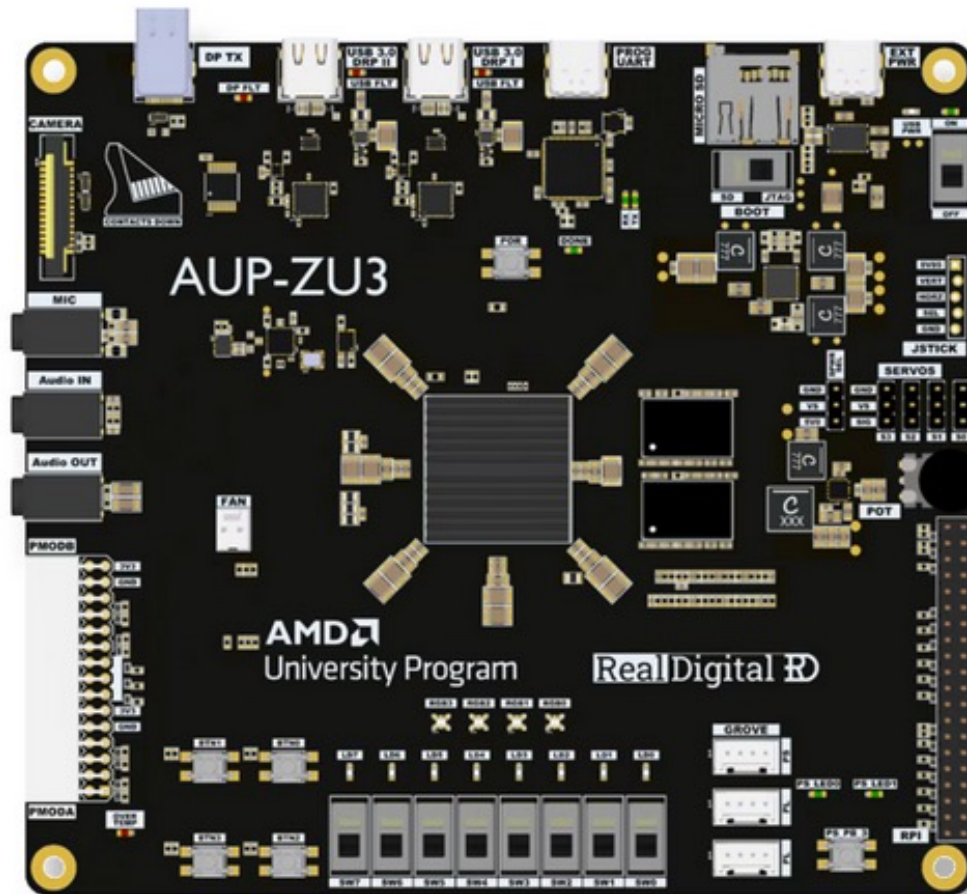# AMD Zynq UltraScale MPSoC for Embedded Systems Design

https://www.amd.com/en/corporate/university
-program/aup-boards/realdigital-aup-zu3.html

Boards courtesy of AMD University Program

UltraScale+ FPGA

Zynq™ UltraScale+™ XCZU3EG-2SFVC784E Features

64-bit Quadcore Arm Cortex-A53 Processors

Dualcore ARM Cortex-R5 Real-Time Processors

Arm Mali™-400MP Graphics Processor

Separate 32 KB L1 caches for instruction and data

Two-stage (hypervisor and guest stages) memory management unit (MMU)

1 MB L2 cache in CCI coherency domain.

Accelerator coherency port (ACP).

128-bit AXI coherency extension (ACE) master interface to CCI

256 KB On-Chip Memory

2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO

2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO on-chip peripherals

71K CLB LUTs
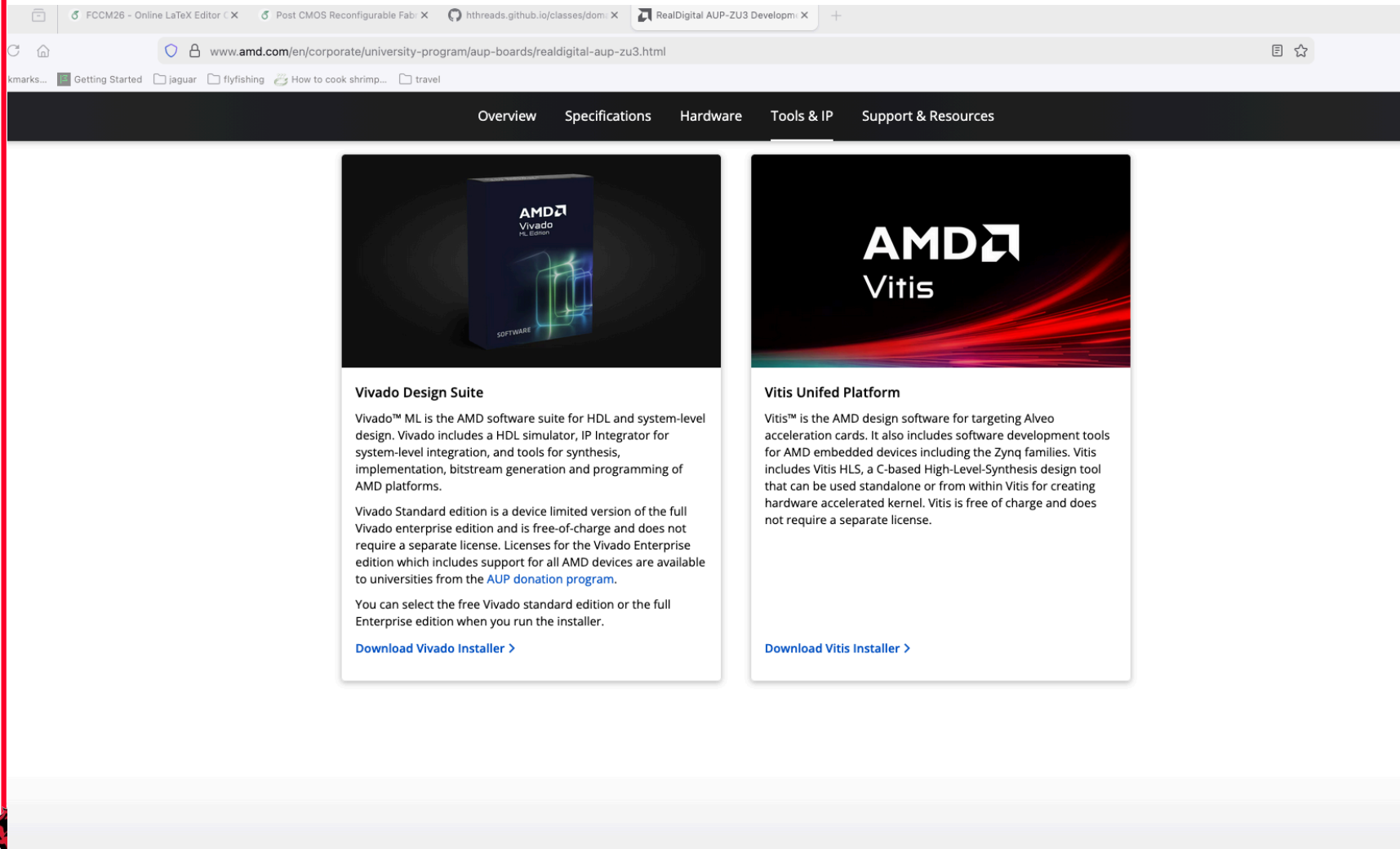
7.6 Mb Block RAM

360 DSP Slices

Three clock management tiles, each with phase-locked loop (PLL)

Internal clock speeds exceeding 450MHz

2x 12 bit, 1 MSPS On-chip analog-to-digital converter (XADC)

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Documentation [↗]

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