

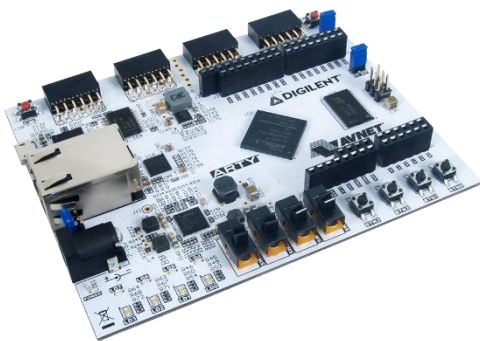
Arty™ FPGA Board Reference Manual

Revised June 7, 2017

This manual applies to the Arty Rev. C

Overview

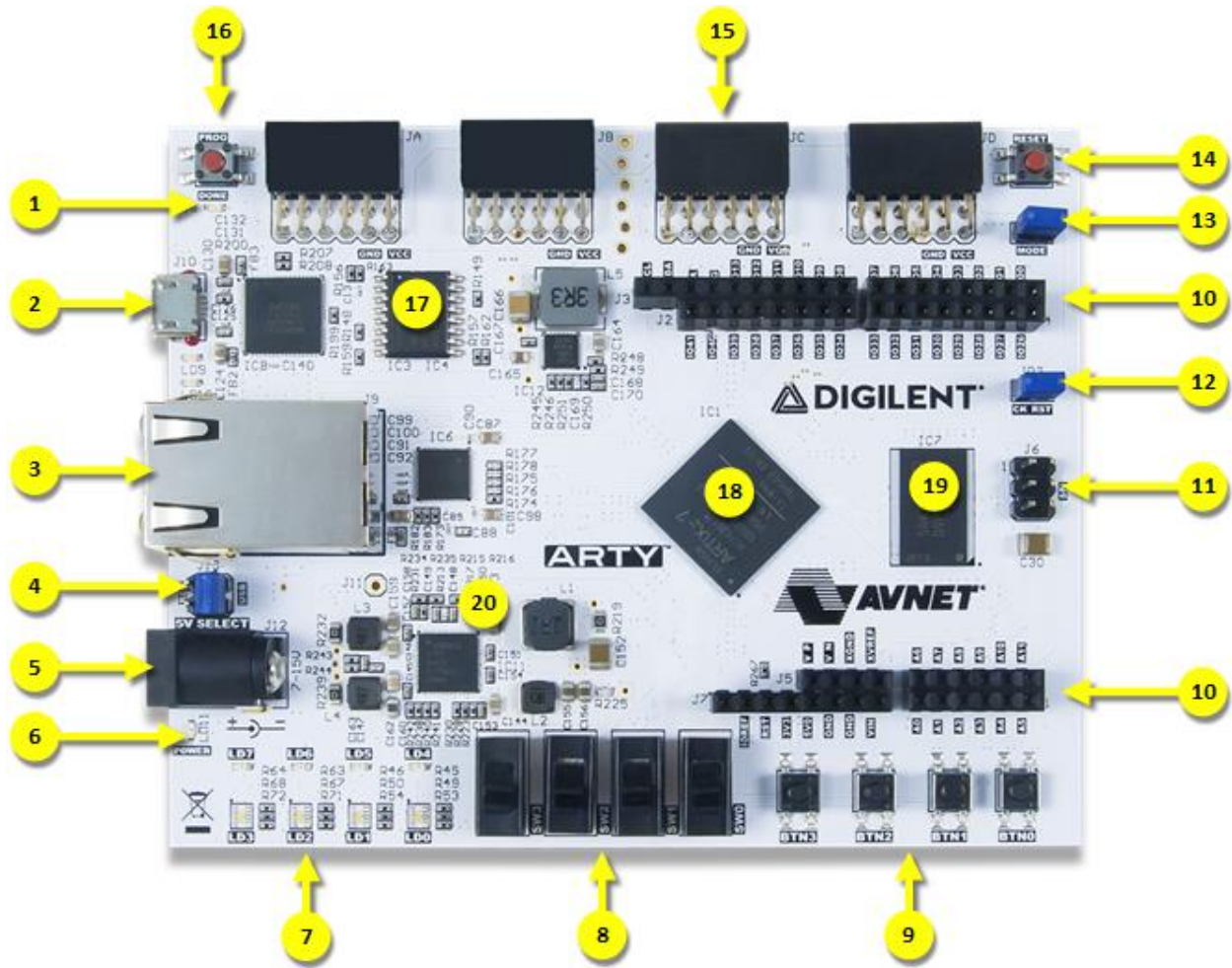
Arty is a ready-to-use development platform designed around the Artix-7 Field Programmable Gate Array (FPGA) from Xilinx. It was designed specifically for use as a MicroBlaze Soft Processing System. When used in this context, Arty becomes the most flexible processing platform you could hope to add to your collection, capable of adapting to whatever your project requires. Unlike other Single Board Computers, Arty isn't bound to a single set of processing peripherals: One moment it's a powerhouse chock-full of UARTS, SPIs, IICs, and an Ethernet MAC, and the next it's a meticulous timekeeper with a dozen 32-bit timers.



The Arty board.

- Xilinx Artix-35T FPGA (xc7a35ticsg324-1L)
 - 33,280 logic cells in 5200 slices (each slice contains four 6-input LUTs and 8 flip-flops);
 - 1,800 Kbits of fast block RAM;
 - Five clock management tiles, each with a phase-locked loop (PLL);
 - 90 DSP slices;
 - Internal clock speeds exceeding 450MHz;
 - On-chip analog-to-digital converter (XADC).
 - Programmable over JTAG and Quad-SPI Flash
- System Features
 - 256MB DDR3L with a 16-bit bus @ 667MHz
 - 16MB Quad-SPI Flash
 - USB-JTAG Programming circuitry
 - Powered from USB or any 7V-15V source
- System Connectivity
 - 10/100 Mbps Ethernet
 - USB-UART Bridge
- Interaction and Sensory Devices
 - 4 Switches
 - 4 Buttons
 - 1 Reset Button
 - 4 LEDs
 - 4 RGB LEDs
- Expansion Connectors
 - 4 Pmod connectors
 - Arduino/chipKIT Shield connector

Arty is fully compatible with the high-performance Vivado[®] Design Suite. It is supported under the free WebPACK[™] license, so designs can be implemented at no additional cost. This free license includes the ability to create MicroBlaze[™] soft-core processor designs. Design resources, example projects, and tutorials are available for download at the Arty Resource Center, accessible from reference.digilentinc.com.



Callout	Description	Callout	Description
1	FPGA programming DONE LED	11	SPI header (Arduino/chipKIT compatible)
2	Shared USB JTAG/UART port	12	chipKIT processor reset jumper
3	Ethernet connector	13	FPGA programming mode (JTAG/Flash)
4	Power select jumper (Ext. supply/USB)	14	chipKIT processor reset
5	Power jack (for optional ext. supply)	15	Pmod headers
6	Power good LED	16	FPGA programming reset button
7	User LEDs	17	SPI Flash
8	User slide switches	18	Artix FPGA
9	User push-buttons	19	Micron DDR3 memory
10	Arduino/chipKIT shield connectors	20	Analog devices ADP 5052 power supply

Table 1. Arty hardware callout descriptions.

2 Designing with Arty

What makes Arty so flexible is its FPGA. Among their many features, FPGAs have the ability to transform into a custom software-defined System-on-a-Chip (SoC). These “Soft SoC” FPGA configurations are designed graphically using a tool called Vivado IP Integrator (Vivado IPI). In this tool, pre-built peripheral blocks are dragged from an extensive library and dropped into your processing system as you see fit. These pre-built peripherals include timers, UART/SPI/IIC controllers, and many of the other devices you would typically find in an SoC or microcontroller. Ambitious users will also find that they can create their own peripheral blocks by writing them in a Hardware Definition Language (HDL), specifically Verilog or VHDL. For those with no interest in learning HDL, the Xilinx High Level Synthesis tool can be used to define custom peripheral blocks by writing them in C.

Arty's Soft SoC configurations are powered by MicroBlaze processor cores. MicroBlaze is a 32-bit RISC soft processor core, designed specifically to be used in Xilinx FPGAs. The MicroBlaze processor in an Arty SoC configuration is typically run at 100 MHz, though it is possible to design your SoC so that it can operate at over 200MHz. Arty supports large MicroBlaze programs with demanding memory requirements by providing 16MB of non-volatile program memory and 256MB of DDR3L RAM.

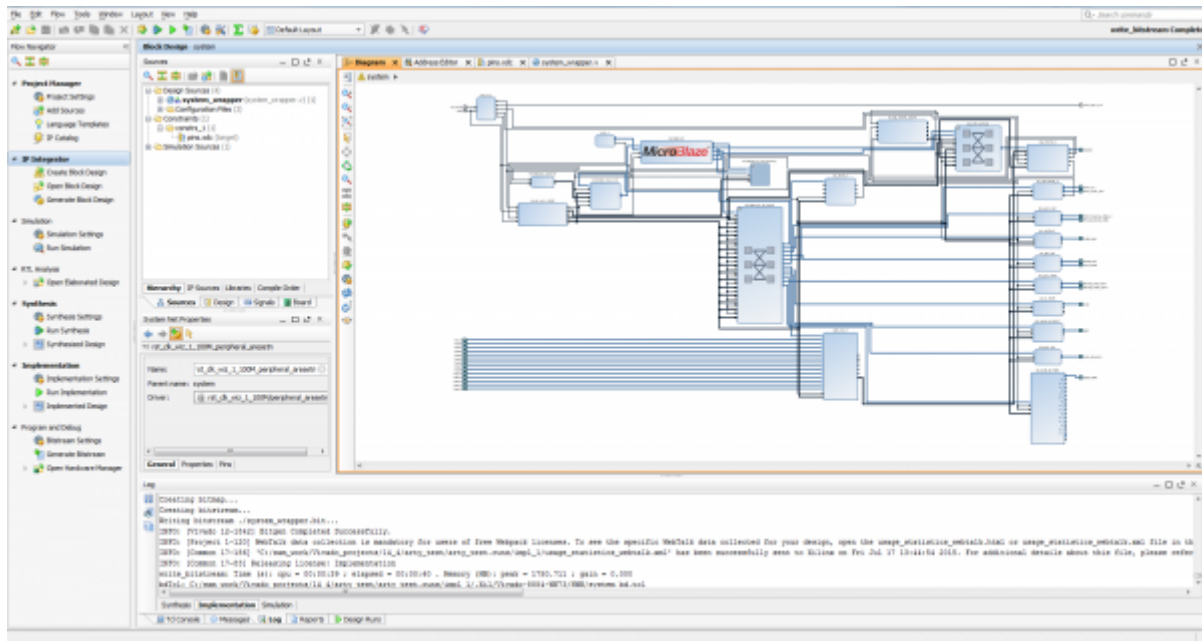


Figure 2.1. Vivado IPI.

After you design your soft SoC configuration for Arty you can start writing programs for it. This is done by exporting your SoC design out of Vivado IPI and into the Xilinx Software Development Kit (XSDK), an Integrated Development Environment (IDE) for designing/debugging MicroBlaze programs in C. After the IPI to XSDK handoff, XSDK is automatically configured to include libraries and examples for the peripheral blocks you've included in your SoC. At this point, programming the Arty is very similar to programming other SoC or microcontroller platforms: Programs are written in C, programmed into board over USB, and then optionally debugged in hardware. Soft SoC configurations and MicroBlaze programs can also be loaded into the 16MB non-volatile program memory so that they execute immediately after Arty is powered on.

Although the Arty is particularly well suited for MicroBlaze Soft SoC designs, it can also be programmed with a Register-Transfer Level (RTL) circuit description like any other FPGA development platform. This design flow requires that you describe your RTL circuit using an HDL within Vivado, and it does not use the Vivado IPI or XSDK tools. Designing this way has many advantages, but is very unlike programming a single board computer, and

instead is used by those familiar with FPGA design or interested in designing and implementing a digital circuit that doesn't contain a processor.

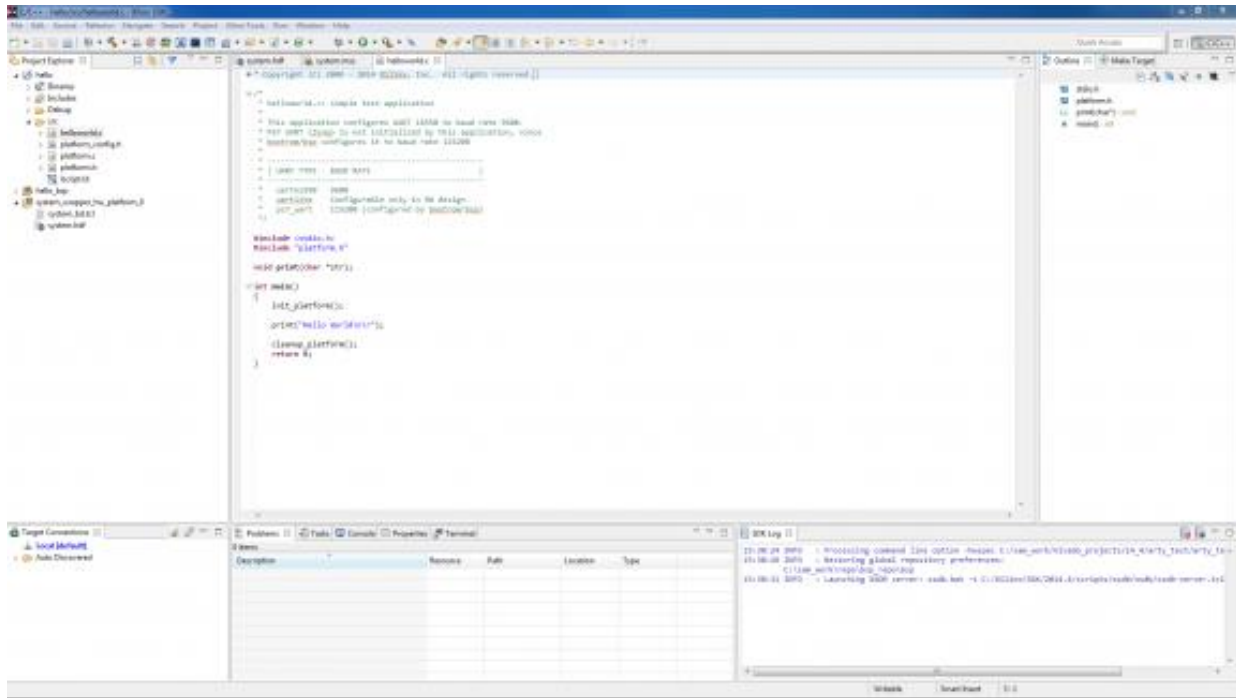


Figure 2.2. Xilinx Software Development Kit (XSDK).

3 Power Supplies

The Arty board requires a 5V power source to operate. This power source can come from the Digilent USB-JTAG port (J10) or it can be derived from a 7 to 15 Volt DC power supply that’s connected to Power Jack (J12) or Pin 8 of Header J7. Header J13, located between the power jack and the Ethernet connector, is used to determine which source is used.

A power-good LED (LD11), driven by the “power good” (PWRGD) output of the ADP5052 regulator, indicates that the board is receiving power and that the onboard supplies are functioning as expected. An overview of the Arty power circuit is shown below.

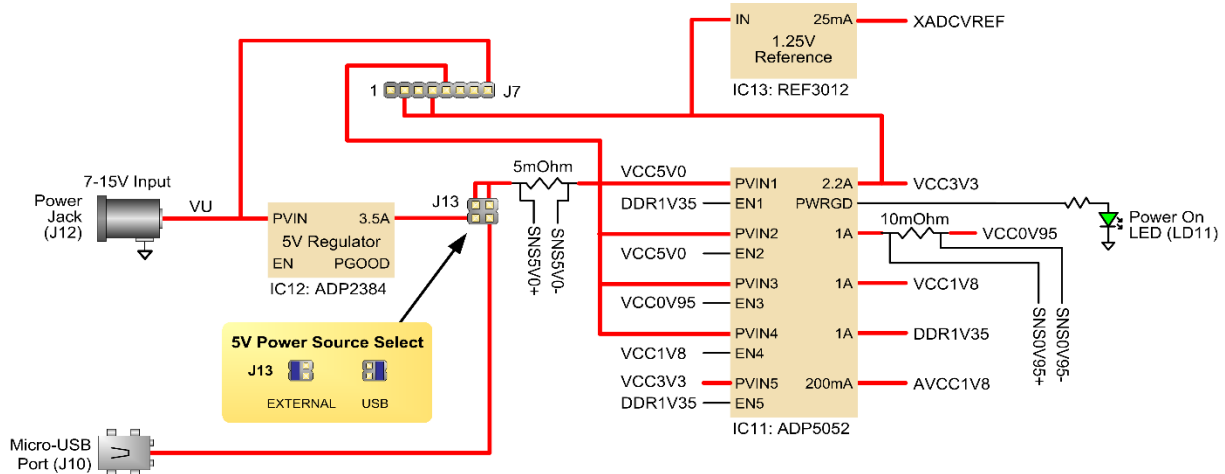


Figure 3.1. Arty power circuit.

The USB port can deliver enough power for the vast majority of designs. However, a few demanding applications, including any that drive multiple peripheral boards, might require more power than the USB port can provide. Also, some applications may need to run without being connected to a PC's USB port. In these instances, an external power supply or battery pack can be used.

An external power supply can be used by plugging into Power Jack J12 and installing a jumper in the "REG" position on Header J13. The supply must use a coaxial, center-positive 2.1mm (or 2.5mm) internal-diameter plug, and provide a voltage of 7 to 15 Volts DC. The supply should provide a minimum current of 1 amp. Ideally, the supply should be capable of providing 36 Watts of power (12 Volts DC, 3 amps).

An external battery pack can be used by connecting the battery's positive terminal to pin 8 of J7 (labeled VIN) and the negative terminal to pin 7 of J7 (labeled GND), as shown in the figure below. In order to use the battery pack as the board's power source a jumper must be installed in the "REG" position on Header J13. The battery must provide a voltage between 7 and 15 volts DC, and should NOT be installed while there is a supply connected to Power Jack J12.

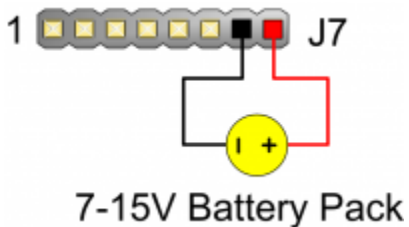


Figure 3.2. Battery pack connection.

Voltage regulator circuits from Analog Devices and Texas Instruments create the required 3.3V, 1.8V, 1.35V, 1.25V, and 0.95V supplies from the 5V power source. In the event that an external supply or battery pack is used, the on-board Analog Devices 5V regulator provides the 5V source. The table below provides additional information (typical currents depend strongly on FPGA configuration and the values provided are typical of medium size/speed designs).

Supply	Circuits	Device	Current (max/typical)
5V	On-board regulators, RGB LEDs	IC12: Analog Devices ADP2384	3.5A/0.375A to 2A
3.3V	FPGA I/O, clocks, flash, Pmods, LEDs, buttons, switches, USB port, Ethernet	IC11: Analog Devices ADP5052	2.2A/NA
0.95V	FPGA Core and Block RAM	IC11: Analog Devices ADP5052	1.0A/0.2A to 0.8A
1.8V	FPGA Auxiliary	IC11: Analog Devices ADP5052	1.0A/NA
1.35V	DDR3L and associated FPGA bank	IC11: Analog Devices ADP5052	1.0A/NA
1.25V	XADC analog reference	IC13: Texas Instruments REF3012	25mA/NA

Table 2. Voltage regulator circuit information.

3.1 External Supply Voltage Monitoring

The Arty board includes circuitry for monitoring the voltage of an external supply connected to Power Jack J12, or an external battery pack connected to header J7. A voltage divider is used to scale the unregulated input voltage, V_U , to be within the range (0-1V) that the on-chip 12-bit ADC is capable of measuring. The unregulated input voltage, V_U , is divided by 16 and then fed into Auxiliary Channel 2 on the XADC of the Artix 35T. Applications that

wish to monitor the voltage of an external supply may configure Channel 2 of the XADC as a unipolar input and perform a conversion to receive a digital value corresponding to the input voltage. The figure below provides an overview that allows an external supply voltage to be monitored.

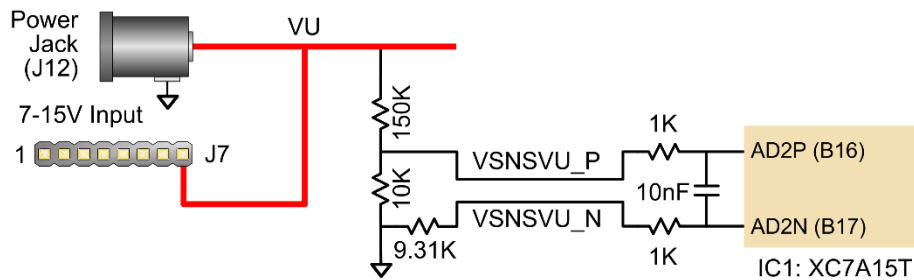


Figure 3.1.1. Monitoring external voltage supply.

3.2 FPGA Core Supply Current Monitoring

The Arty board includes circuitry for monitoring the current consumed by the FPGA core. The current is monitored by measuring the voltage across a 10 milliohm sense resistor that's placed between the output of the 0.95V switching regulator (IC11, Channel 2) and the VCC0V95 network. A current sense amplifier (IC15, Texas Instrument's INA199A1) connected across the sense resistor provides a gain of 50 and produces an output voltage of 500 millivolts per amp of current. The output of the current sense amplifier is fed into Auxiliary Channel 10 on the XADC of the Artix 35T. Applications that wish to monitor the current consumption of the FPGA Core and Block RAM may configure Channel 10 of the XADC as a unipolar input and perform a conversion to receive a digital value that corresponds to the amplified sense resistor voltage. The figure below provides an overview of the circuitry that allows the FPGA Core Supply current to be monitored.

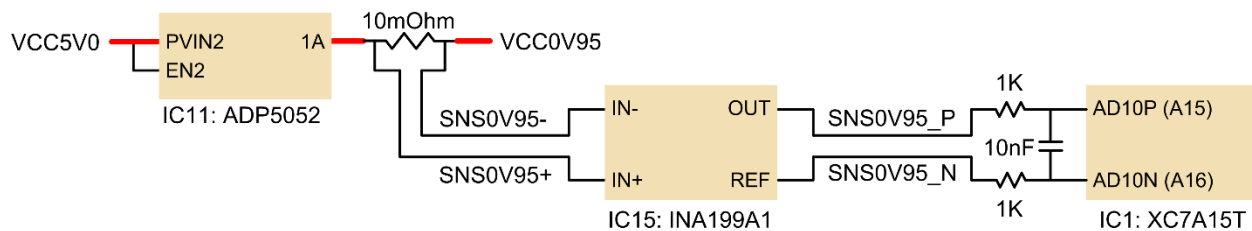


Figure 3.2.1. FPGA core supply current monitoring.

3.3 5V Supply Power Monitoring

The Arty board includes circuitry for monitoring the voltage of the 5 Volt supply as well as the current consumed from this supply. A voltage divider is used to scale the 5V input voltage to be within the range (0-1V) that the on-chip 12-bit ADC is capable of measuring. The 5V supply voltage is divided by 5.99 and then fed into auxiliary Channel 1 on the XADC of the Artix 35T. A combination of a 5 milliohm current sense resistor and a current sense amplifier (IC14, Texas Instruments INA199A1) are used to produce an output voltage of 250 millivolts per amp of current. The output of the current sense amplifier is fed into Auxiliary channel 9 on the XADC of the Artix 35T. Applications that wish to monitor the instantaneous power consumption of the Arty board may configure Channels 1 and 9 of the XADC as unipolar inputs and then perform a simultaneous conversion of the two channels to receive digital values that can be used to compute the instantaneous power consumption. The figure below provides an overview of the circuitry that allows the 5V Supply power consumption to be monitored.

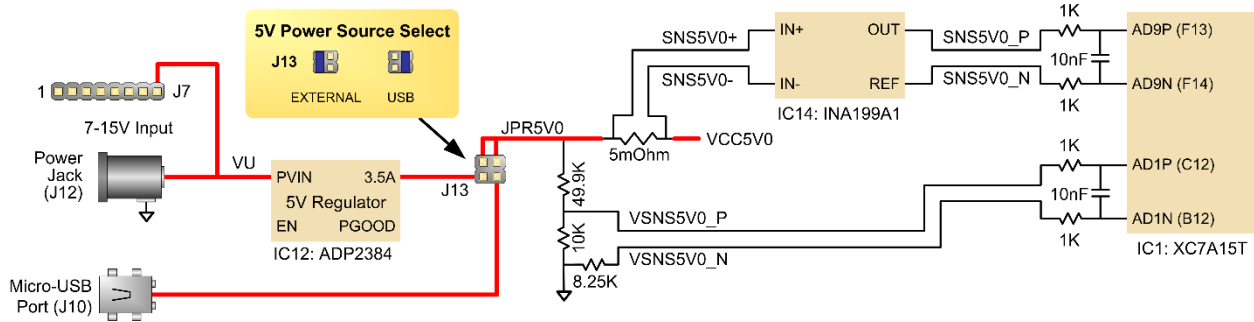


Figure 3.3.1. 5V supply power consumption.

4 FPGA Configuration

After power-on, the Artix-7 FPGA must be configured (or programmed) before it can perform any function. You can configure the FPGA in one of two ways:

1. A PC can use the Digilent USB-JTAG circuitry (port J10) to program the FPGA any time the power is on.
2. A file stored in the nonvolatile serial (SPI) flash device can be transferred to the FPGA using the SPI port.

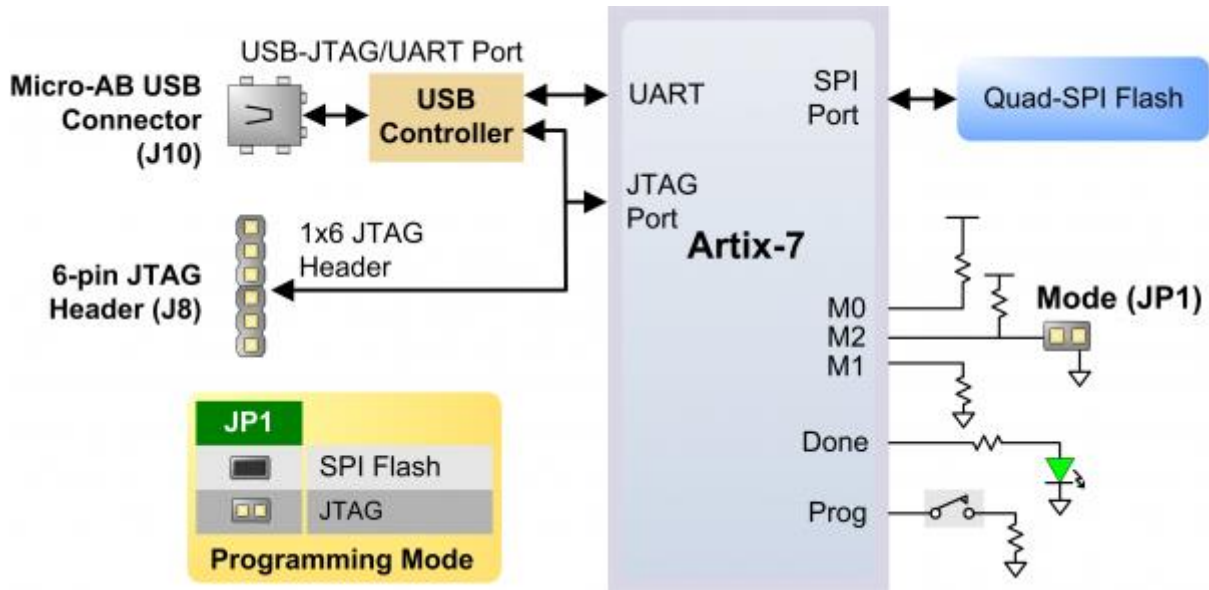


Figure 4.1. Arty configuration.

Figure 3 shows the different options available for configuring the FPGA. An on-board “mode” jumper (JP1) selects whether the FPGA will be programmed by the Quad-SPI flash on power up.

The FPGA configuration data is stored in files called bitstreams that have the .bit file extension. The ISE or Vivado software from Xilinx can create bitstreams from VHDL, Verilog, or schematic-based source files (in the ISE toolset, EDK is used for MicroBlaze embedded processor-based designs).

Bitstreams are stored in volatile memory cells within the FPGA. This data defines the FPGA’s logic functions and circuit connections, and it remains valid until it is erased by removing board power, by pressing the reset button attached to the PROG input, or by writing a new configuration file using the JTAG port.

An Artix-7 35T bitstream is typically 17,536,096 bits. The time it takes to program the Arty can be decreased by compressing the bitstream before programming, and then allowing the FPGA to decompress the bitstream itself during configuration. Depending on design complexity, compression ratios of 10x can be achieved. Bitstream compression can be enabled within the Xilinx tools (ISE or Vivado) to occur during generation. For instructions on how to do this, consult the Xilinx documentation for the toolset being used.

After being successfully programmed, the FPGA will cause the “DONE” LED to illuminate. Pressing the “PROG” button at any time will reset the configuration memory in the FPGA. After being reset, the FPGA will immediately attempt to reprogram itself from whatever method has been selected by the programming mode jumpers.

The following sections provide greater detail about programming the Arty using the different methods available.

4.1 JTAG Configuration

The Xilinx tools typically communicate with FPGAs using the Test Access Port and Boundary-Scan Architecture, commonly referred to as JTAG. During JTAG programming, a .bit file is transferred from the PC to the FPGA using the onboard Digilent USB-JTAG circuitry (port J10) or an external JTAG programmer, such as the Digilent JTAG-HS2, attached to port J8. You can perform JTAG programming any time after the Arty has been powered on, regardless of whether the mode jumper (JP1) is set. If the FPGA is already configured, then the existing configuration is overwritten with the bitstream being transmitted over JTAG. Not setting the mode jumper (seen in Figure 3) is useful to prevent the FPGA from being configured from Quad-SPI Flash until a JTAG programming occurs.

Programming the Arty with an uncompressed bitstream using the on-board USB-JTAG circuitry usually takes around 6 seconds. JTAG programming can be done using the hardware manager in Vivado or the iMPACT tool included with ISE.

4.2 Quad-SPI Configuration

Since the FPGA's memory on the Arty is volatile, it relies on the Quad-SPI flash memory to store the configuration between power cycles. This configuration mode is called Master SPI. The blank FPGA takes the role of master and reads the configuration file out of the flash device upon power-up. To that effect, a configuration file needs to be downloaded first to the flash. When programming a nonvolatile flash device, a bitstream file is transferred to the flash in a two-step process. First, the FPGA is programmed with a circuit that can program flash devices, and then data is transferred to the flash device via the FPGA circuit (this complexity is hidden from the user by the Xilinx tools). This is called indirect programming. After the flash device has been programmed, it can automatically configure the FPGA at a subsequent power-on or reset event as determined by the mode jumper setting (see Figure 3). Programming files stored in the flash device will remain until they are overwritten, regardless of power-cycle events.

Programming the flash can take as long as four to five minutes, which is mostly due to the lengthy erase process inherent to the memory technology. Once written however, FPGA configuration can be very fast—less than a second. Bitstream compression, SPI bus width, and configuration rate are factors controlled by the Xilinx tools that can affect configuration speed. The Arty supports x1, x2, and x4 bus widths and data rates of up to 50 MHz for Quad-SPI programming.

Quad-SPI programming can be done using the hardware manager in Vivado or with the iMPACT tool included with ISE.

5 Memory

The Arty board contains two external memories: a 256MB DDR3L SDRAM and a 128Mb (16MB) non-volatile serial flash device. The DDR3L module is connected to the FPGA using the industry standard interface. The serial flash is on a dedicated quad-mode (x4) SPI bus. The connection and a pin assignment between the FPGA and external memories are shown below.

5.1 DDR3L

The Arty includes one MT41K128M16JT-125 memory component, creating a single rank, 16-bit wide interface. It is routed to a 1.35V-powered HR (High Range) FPGA bank with 50 ohm controlled single-ended trace impedance. 50 ohm internal terminations in the FPGA are used to match the trace characteristics. Similarly, on the memory side, on-die terminations (ODT) are used for impedance matching.

For proper operation of the memory, a memory controller and physical layer (PHY) interface needs to be included in the FPGA design. The easiest way to accomplish this on the Arty is to use the Xilinx 7-series memory interface solutions core generated by the MIG (Memory Interface Generator) Wizard. Depending on the tool used (ISE, EDK or Vivado), the MIG Wizard can generate a native FIFO-style or an AXI4 interface to connect to user logic. This workflow allows the customization of several DDR parameters optimized for the particular application. Table 2 below lists the MIG Wizard settings optimized for the Arty.

Setting	Value
Memory type	DDR3 SDRAM
Max clock period	3000ps (667Mbps data rate)
Memory part	MT41K128M16XX-15E
Memory voltage	1.35V
Data width	16
Data mask	Enabled
Recommended input clock period	6000ps (166.667 MHz)
Output driver impedance control	RZQ/6
Controller chip select pin	Enabled
Rtt (nominal) – on-die termination	RZQ/6
Interval Vref	Enabled
Internal termination impedance	50omhs

Table 3. DDR3L settings for the Arty.

The MIG Wizard will require the fixed pin-out of the memory signals to be entered and validated before generating the IP core. For your convenience, an importable UCF file is provided on the Arty resource center to speed up this process. It is included in the “MIG Project” design resource download. This download also includes a .prj file that can be imported into the wizard to automatically configure it with the options found in Table 2.

For more details on the Xilinx MIG, refer to the 7 Series FPGAs Memory Interface Solutions User Guide (ug586).

5.2 Quad-SPI Flash

FPGA configuration files can be written to the Quad-SPI Flash (Micron part number N25Q128A13ESF40), and setting the mode jumper will cause the FPGA to automatically read a configuration from this device at power on. An Artix-7 35T configuration file requires 17,536,096 bits of memory, leaving about 87% of the flash device (or ~14MB) available for user data. A common use for this extra memory is to store MicroBlaze programs too big to fit in the onboard Block memory (typically 128 KB). These programs are then loaded and executed using a smaller bootloader program that can fit in the block memory. It is possible to automatically generate this bootloader, roll it into a single file (called an .mcs file) that also contains the bitstream and your custom MicroBlaze application, and program this file into SPI Flash using Xilinx SDK and Vivado. Xilinx Answer Record 63605 explains how to do this.

The contents of the memory can be manipulated by issuing certain commands on the SPI bus. The implementation of this protocol is outside the scope of this document. All signals in the SPI bus are general-purpose user I/O pins after FPGA configuration. On other boards, SCK is an exception because it remains a dedicated pin even after configuration, however, on Arty the SCK signal is routed to an additional general purpose pin that can be accessed after configuration (see Figure below). This allows access to this pin without having to instantiate the special FPGA primitive called STARTUPE2.

Xilinx's AXI Quad SPI core can be used to read/write the flash in a MicroBlaze design. Refer to Xilinx's product guide for this core to learn more about using it, or to Micron's datasheet for the flash device to learn how to implement a custom controller.

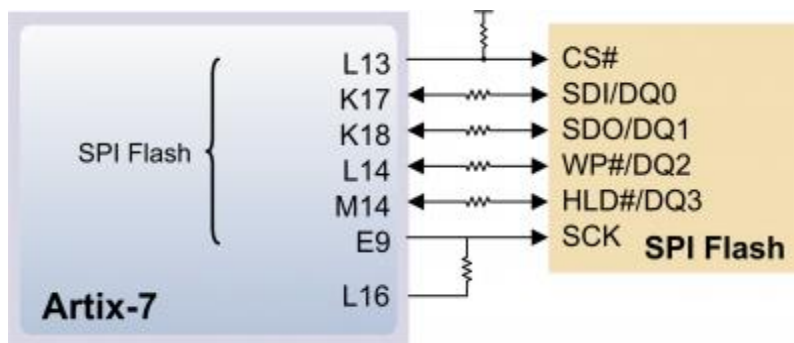


Figure 5.1. Arty SPI flash.

6 Ethernet PHY

Arty includes a Texas Instruments 10/100 Ethernet PHY (TI part number DP83848J) paired with an RJ-45 Ethernet jack with integrated magnetics and indicator LEDs. The TI PHY uses the MII interface and supports 10/100 Mb/s. Figure 5 illustrates the pin connections between the Artix-7 and the Ethernet PHY. At power-on reset, the PHY is set to the following defaults:

- MII mode interface
- Auto-negotiation enabled, advertising all 10/100 mode capable
- PHY address=00001
- LED Mode 2

Two LEDs found in the Ethernet connector (J9) are connected to the PHY to provide link status and data activity feedback. See the PHY datasheet for details. Note that it is normal for one LED to be illuminated and one to be off, even when not using the Ethernet PHY.

Vivado IPI-based designs can access the PHY using either the AXI EthernetLite IP core, the AXI 1G/2.5G Ethernet Subsystem IP core, or the Tri Mode Ethernet MAC IP core. A 25 MHz clock needs to be generated for the X1 pin of the external PHY, labeled ETH_REF_CLK in the Arty Schematic. To learn how to properly use the Ethernet PHY in a MicroBlaze design on the Arty, refer to the [Getting Started with MicroBlaze Servers](#) tutorial from the Arty Resource Center.

For further information on the Ethernet PHY, refer to the DP83848J datasheet.

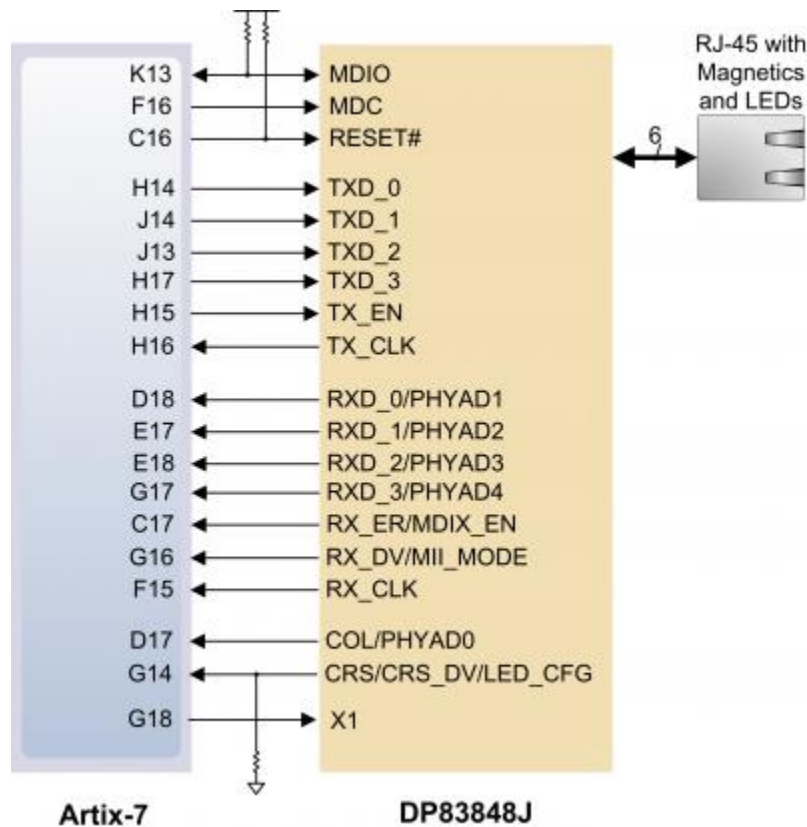


Figure 6.1. Arty Ethernet.

7 Oscillators/Clocks

The Arty board includes a single 100 MHz crystal oscillator connected to pin E3 (E3 is a MRCC input on bank 35). The input clock can drive MMCMs or PLLs to generate clocks of various frequencies and with known phase relationships that may be needed throughout a design. Some rules restrict which MMCMs and PLLs may be driven by the 100 MHz input clock. For a full description of these rules and of the capabilities of the Artix-7 clocking resources, refer to the “7 Series FPGAs Clocking Resources User Guide” available from Xilinx.

Xilinx offers the Clocking Wizard IP core to help users generate the different clocks required for a specific design. This wizard will properly instantiate the needed MMCMs and PLLs based on the desired frequencies and phase relationships specified by the user. The wizard will then output an easy-to-use wrapper component around these clocking resources that can be inserted into the user’s design. The clocking wizard can be accessed from within the Project Navigator or Core Generator tools.

8 USB-UART Bridge (Serial Port)

The Arty includes an FTDI FT2232HQ USB-UART bridge (attached to connector J10) that allows you use PC applications to communicate with the board using standard Windows COM port commands. Free USB-COM port drivers, available from www.ftdichip.com under the “Virtual Com Port” or VCP heading, convert USB packets to UART/serial port data. Serial port data is exchanged with the FPGA using a two-wire serial port (TXD/RXD). After the drivers are installed, I/O commands can be used from the PC directed to the COM port to produce serial data traffic on the A9 and D10 FPGA pins.

Two on-board status LEDs provide visual feedback on traffic flowing through the port: the transmit LED (LD10) and the receive LED (LD9). Signal names that imply direction are from the point-of-view of the DTE (Data Terminal Equipment), in this case the PC.

The FT2232HQ is also used as the controller for the Digilent USB-JTAG circuitry, but the USB-UART and USB-JTAG functions behave entirely independent of one another. Programmers interested in using the UART functionality of the FT2232 within their design do not need to worry about the JTAG circuitry interfering with the UART data transfers, and vice-versa. The combination of these two features into a single device allows the Arty to be programmed, communicated with via UART, and powered from a computer attached with a single Micro USB cable.

The CK_RST signal (see the Arty Schematic) is also connected to the FT2232HQ device via JP2. When JP2 is shorted, the FT2232HQ can trigger a MicroBlaze reset, mimicking the behavior of Arduino and chipKIT boards when sketches are loaded. Note the CK_RST signal is also connected to the red RESET button and the RST pin of J7 on the shield connector (these connections are not shown in the figure below).

The connections between the FT2232HQ and the Artix-7 are shown in Figure 6.

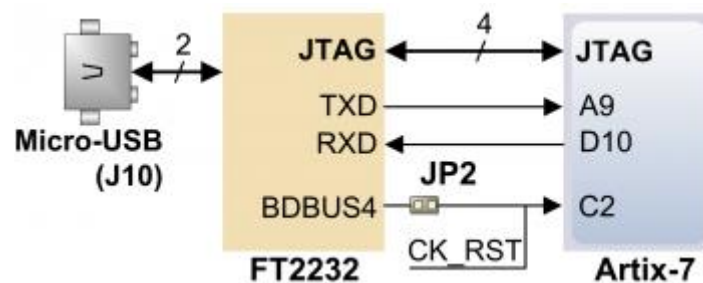


Figure 8.1. UART.

9 Basic I/O

The Arty board includes four tri-color LEDs, 4 switches, 4 push buttons, 4 individual LEDs, and a reset button, as shown in Figure 16. The push buttons and slide switches are connected to the FPGA via series resistors to prevent damage from inadvertent short circuits (a short circuit could occur if an FPGA pin assigned to a push button or slide switch was inadvertently defined as an output). The four push buttons are “momentary” switches that normally generate a low output when they are at rest, and a high output only when they are pressed. Slide switches generate constant high or low inputs depending on their position.

The red reset button labeled “RESET” generates a high output when at rest and a low output when pressed. The RESET button is intended to be used in MicroBlaze designs to reset the processor, but you can also use it as a

general purpose push button. Note that it is also tied to the RST pin on J7 of the shield connector and to the FT2232 UART device via JP2, though these connections are not shown in the figure below.

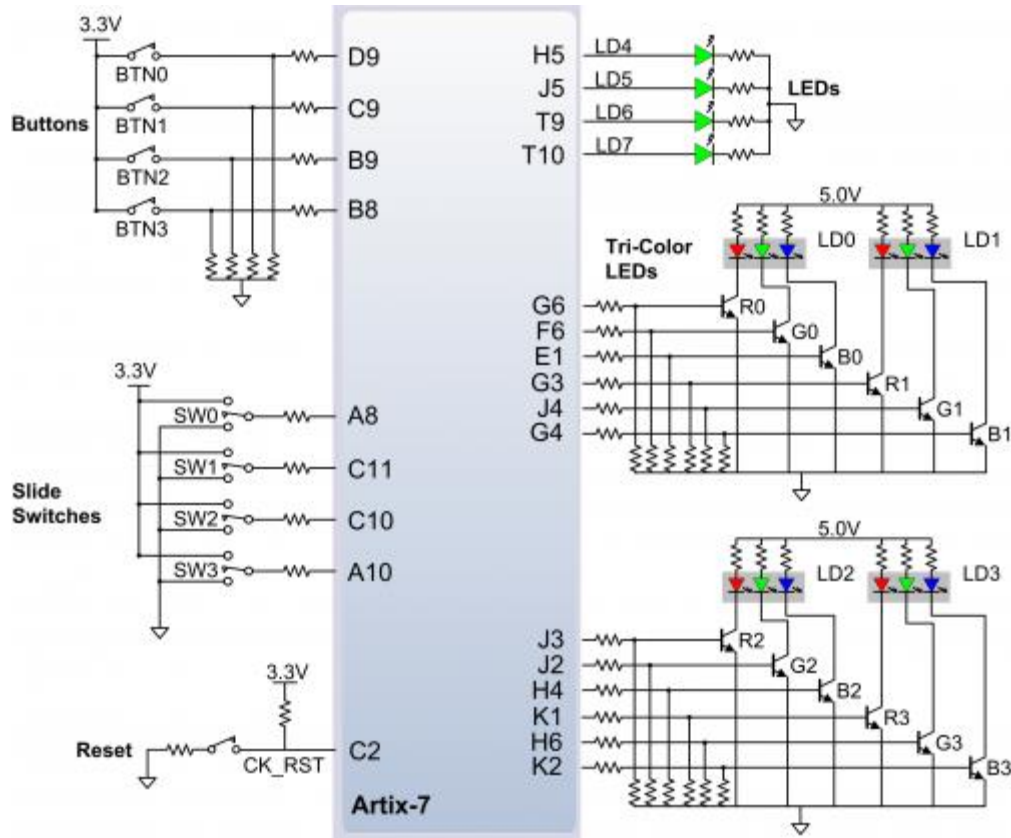


Figure 9.1. Arty GPIO.

The four individual high-efficiency LEDs are anode-connected to the FPGA via 330-ohm resistors, so they will turn on when a logic high voltage is applied to their respective I/O pin. Additional LEDs that are not user-accessible indicate power-on, FPGA programming status, and USB and Ethernet port status.

9.1 Tri-color LEDs

The Arty board contains four tri-color LEDs. Each tri-color LED has three input signals that drive the cathodes of three smaller internal LEDs: one red, one blue, and one green. Driving the signal corresponding to one of these colors high will illuminate the internal LED. The input signals are driven by the FPGA through a transistor, which inverts the signals. Therefore, to light up the tri-color LED, the corresponding signals need to be driven high. The tri-color LED will emit a color dependent on the combination of internal LEDs that are currently being illuminated. For example, if the red and blue signals are driven high and green is driven low, the tri-color LED will emit a purple color.

Note: Digilent strongly recommends the use of pulse-width modulation (PWM) when driving the tri-color LEDs. Driving any of the inputs to a steady logic '1' will result in the LED being illuminated at an uncomfortably bright level. You can avoid this by ensuring that none of the tri-color signals are driven with more than a 50% duty cycle. Using PWM also greatly expands the potential color palette of the tri-color led. Individually adjusting the duty cycle of each color between 50% and 0% causes the different colors to be illuminated at different intensities, allowing virtually any color to be displayed.

10 Pmod Connectors

Pmod connectors are 2×6, right-angle, 100-mil spaced female connectors that mate with standard 2×6 pin headers. Each 12-pin Pmod connector provides two 3.3V VCC signals (pins 6 and 12), two Ground signals (pins 5 and 11), and eight logic signals, as shown in Fig. 16. The VCC and Ground pins can deliver up to 1A of current, but care must be taken not to exceed any of the power budgets of the onboard regulators or the external power supply (these are described in the “Power supplies” section).

Digilent produces a large collection of Pmod accessory boards that can attach to the Pmod expansion connectors to add ready-made functions like A/D’s, D/A’s, motor drivers, sensors, and other functions.

The Arty has four Pmod connectors, some of which behave differently than others. Each Pmod connector falls into one of two categories: standard or high-speed. Table 9 specifies which category each Pmod falls into, and also lists the FPGA pins they are connected to. The following sections describe the different types of Pmods.

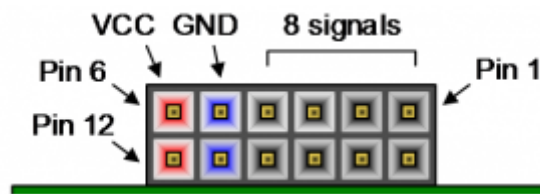


Figure 10.1. Pmod connector.

	Pmod JA	Pmod JB	Pmod JC	Pmod JD
Pmod Type	Standard	High-speed	High-speed	Standard
Pin 1	G13	E15	U12	D4
Pin 2	B11	E16	V12	D3
Pin 3	A11	D15	V10	F4
Pin 4	D12	C15	V11	F3
Pin 7	D13	J17	U14	E2
Pin 8	B18	J18	V14	D2
Pin 9	A18	K15	T13	H2
Pin 10	K16	J15	U13	G2

Table 4. Pmod connector categories.

10.1 Standard Pmod

The standard Pmod connectors are connected to the FPGA via 200Ohm series resistors. The series resistors prevent short circuits that can occur if the user accidentally drives a signal that is supposed to be used as an input. The downside to this added protection is that these resistors can limit the maximum switching speed of the data signals. If the Pmod being used does not require high-speed access, then the standard Pmod connector should be used to help prevent damage to the devices.

Pin Name	Shield Function	Arty Connection
IO0-IO13, IO26-IO41, A (IO42)	General purpose I/O pins	See Section titled “Shield Digital I/O”
SCL	I2C clock	See Section titled “Shield Digital I/O”
SDA	I2C data	See Section titled “Shield Digital I/O”
SCLK	SPI clock	See Section titled “Shield Digital I/O”
MOSI	SPI data out	See Section titled “Shield Digital I/O”
MISO	SPI data in	See Section titled “Shield Digital I/O”
SS	SPI slave select	See Section titled “Shield Digital I/O”
A0-A5	Single-ended analog input	See Section titled “Shield Digital I/O”
A6-A11	Differential analog input	See Section titled “Shield Digital I/O”
V_P, V_N	Dedicated differential analog input	See Section titled “Shield Digital I/O”
XGND	XADC analog ground	Connected to net used to drive the XADC ground reference on the FPGA (VREFN)
XVREF	XADC analog voltage	Connected to 1.25V, 25mA rail used to drive the XADC voltage reference on the FPGA (VREFP)
N/C	Not connected	Not connected
IOREF	Digital I/O voltage reference	Connected to the Arty 3.3V power rail (See the “Power Supplies” section)
RST	Reset to shield	Connected to the red “RESET” button and a digital I/O of the FPGA. When JP2 is shorted, it is also connected to the DTR signal of the FTDI USB-UART bridge.
3V3	3.3V power rail	Connected to the Arty 3.3V power rail (see the “Power Supplies” section)
5V0	5.0V power rail	Connected to the Arty 5.0V power rail (see the “Power Supplies” section)
GND, G	Ground	Connected to the ground plane of Arty
VIN	Power input	Connected in parallel with the external power supply connector (J12). See the “Power Supplies” section for information on powering Arty from this pin.

Table 5. Shield connection table and functional description.

11.1 Shield Digital I/O

The pins connected directly to the FPGA can be used as general purpose inputs or outputs. These pins include the I2C, SPI, and general purpose I/O pins. There are 200 Ohm series resistors between the FPGA and the digital I/O pins to help provide protection against accidental short circuits. The absolute maximum and recommended operating voltages for these pins are outlined in the table below.

	Absolute Minimum Voltage	Recommended Minimum Operating Voltage	Recommended Maximum Operating Voltage	Absolute Maximum Voltage
Powered	-0.4V	-0.2V	3.4V	3.75V
Unpowered	-0.4V	N/A	N/A	0.55V

Table 6. Absolute maximum and recommended operating voltages.

For more information on the electrical characteristics of the pins connected to the FPGA, please see the [Artix-7 datasheet](#) from Xilinx.

11.2 Shield Analog I/O

The pins labeled A0-A11 and V_P/V_N are used as analog inputs to the XADC module of the FPGA. The FPGA expects that the inputs range from 0-1 V. On the pins labeled A0-A5 we use an external circuit to scale down the input voltage from 3.3V. This circuit is shown in Figure 11.2.1. This circuit allows the XADC module to accurately measure any voltage between 0V and 3.3V (relative to the Arty's GND) that is applied to any of these pins. If you wish to use the pins labeled A0-A5 as Digital inputs or outputs, they are also connected directly to the FPGA before the resistor divider circuit (also shown in Figure 11.2.1).

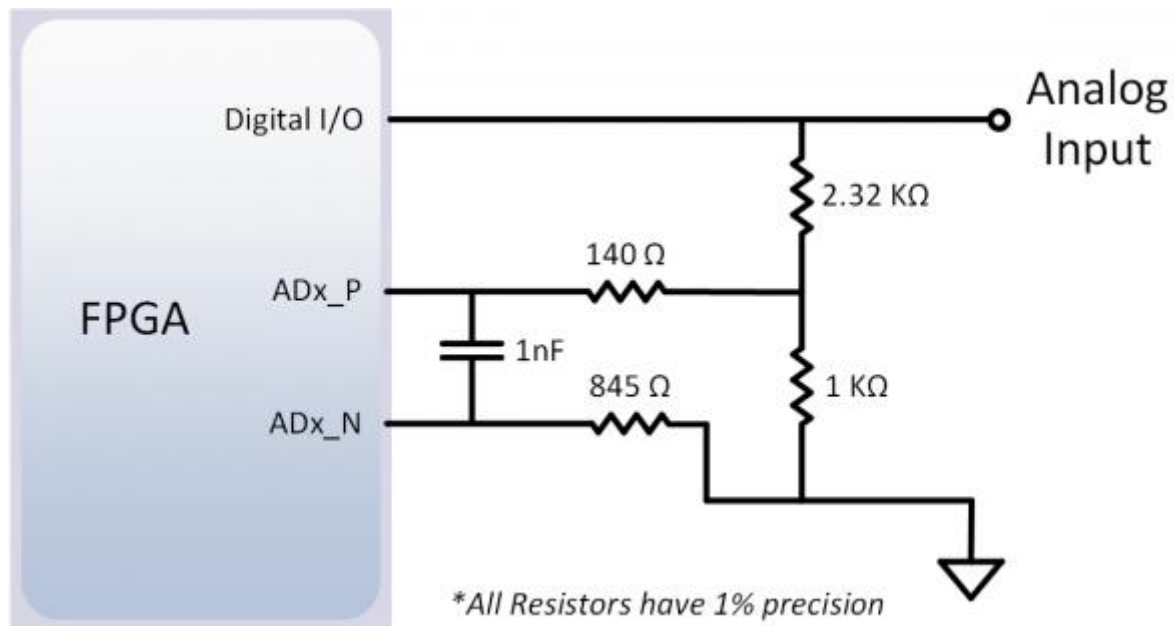


Figure 11.2.1. External circuit.

The pins labeled A6-A11 are connected directly to 3 pairs of analog capable pins on the FPGA via an anti-aliasing filter. This circuit is shown in Figure 11.2.2. These pairs of pins can be used as differential analog inputs with a voltage difference between 0-1V. The even numbers are connected to the positive pins of the pair and the odd numbers are connected to the negative pins (so A6 and A7 form an analog input pair with A6 being positive and A7 being negative). Note that though the pads for the capacitor are present, they are not loaded for these pins. Since the analog capable pins of the FPGA can also be used like normal digital FPGA pins, it is also possible to use these pins for Digital I/O.

The pins labeled V_P and V_N are connected to the VP_0 and VN_0 dedicated analog inputs of the FPGA. This pair of pins can also be used as a differential analog input with voltage between 0-1V, but they cannot be used as Digital I/O. The capacitor in the circuit shown in Figure 11.2.2 for this pair of pins is loaded on the Arty.

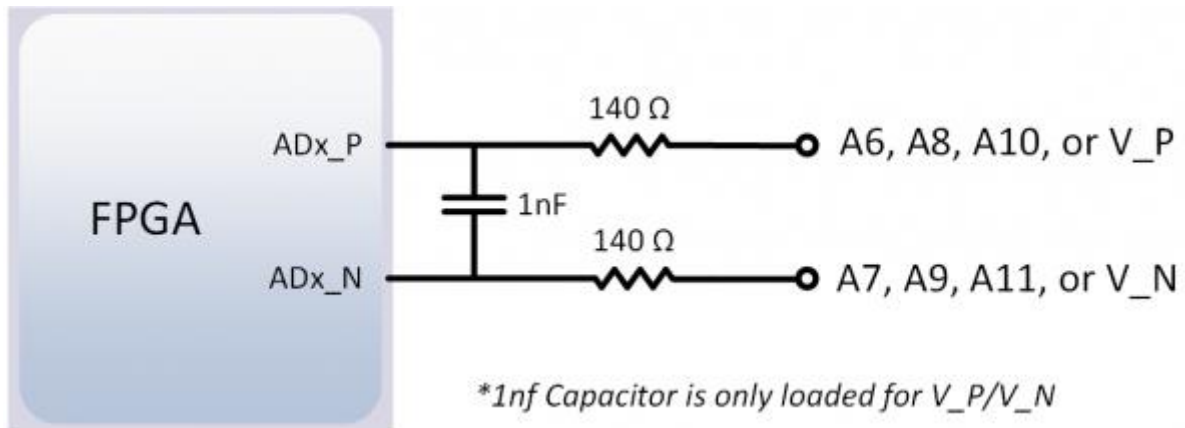


Figure 11.2.2. Dedicated analog inputs.

The XADC core within the Artix-7 is a dual channel 12-bit analog-to-digital converter capable of operating at 1 MSPS. Either channel can be driven by any of the analog inputs connected to the shield pins. The XADC core is controlled and accessed from a user design via the Dynamic Reconfiguration Port (DRP). The DRP also provides access to voltage monitors that are present on each of the FPGA's power rails, and a temperature sensor that is internal to the FPGA. For more information on using the XADC core, refer to the Xilinx document titled 7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter. A demo that uses the XADC core is available on the Arty resource center.