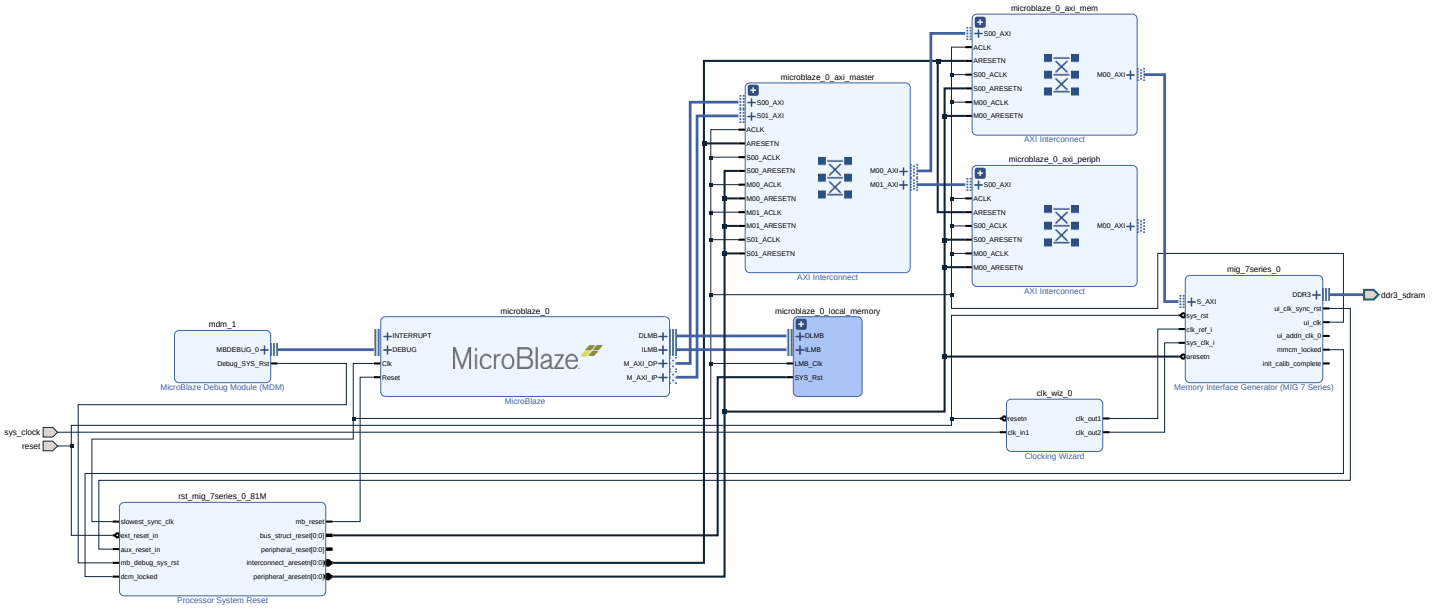
microblaze_0_axi_mem
S00_AXI
ACLK
ARESETN
S00_ACLK
S00_ARESETN
M00_ACLK
M00_ARESETN
M00_AXI
AXI Interconnect
microblaze_0_axi_master
S00_AXI
S01_AXI
ACLK
ARESETN
S00_ACLK
S00_ARESETN
M00_ACLK
M00_ARESETN
M01_ACLK
M01_ARESETN
S01_ACLK
S01_ARESETN
M00_AXI
M01_AXI
AXI Interconnect
microblaze_0_axi_periph
S00_AXI
ACLK
ARESETN
S00_ACLK
S00_ARESETN
M00_ACLK
M00_ARESETN
M00_AXI
AXI Interconnect
mdm_1
MBDEBUG_0
Debug_SYS_Rst
MicroBlaze Debug Module (MDM)
microblaze_0
INTERRUPT
DEBUG
Clk
Reset
MicroBlaze
DLMB
ILMB
M_AXI_DP
M_AXI_IP
microblaze_0_local_memory
DLMB
ILMB
LMB_Clk
SYS_Rst
mig_7series_0
S_AXI
sys_rst
clk_ref_i
sys_clk_i
aresetn
DDR3
ui_clk_sync_rst
ui_clk
ui_addn_clk_0
mmcm_locked
init_calib_complete
Memory Interface Generator (MIG 7 Series)
ddr3_sdram
clk_wiz_0
resetn
clk_in1
clk_out1
clk_out2
Clocking Wizard
sys_clock
reset
rst_mig_7series_0_81M
slowest_sync_clk
ext_reset_in
aux_reset_in
mb_debug_sys_rst
dcm_locked
mb_reset
bus_struct_reset[0:0]
peripheral_reset[0:0]
interconnect_aresetn[0:0]
peripheral_aresetn[0:0]
Processor System Reset